ABSTRACT

A method of forming a gate structure in an integrated circuit on a substrate. A high k layer is formed on the substrate, and a gate electrode layer is formed on the high k layer. The gate electrode layer is the patterned. LDD regions are formed using an ion implantation process, thereby creating damaged portions of the high k layer. A first portion of the damaged portions of the high k layer are removed, thereby defining a gate structure, and leaving remaining portions of the damaged portions of the high k layer. Sidewall spacers are formed adjacent the gate structure. Source/drain regions are formed using an ion implantation process, thereby further damaging the remaining portions of the damaged portions of the high k layer. The remaining portions of the damaged portions of the high k layer are then removed.

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